NiO Resistive Random Access Memory Nanocapacitor Array on Graphene

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ABSTRACT In this study, a NiO RRAM nanocapacitor array was fabricated on a graphene sheet, which was on a Nb-doped $SrTiO_3$ substrate containing terraces with a regular interval of about 100 nm and an atomically smooth surface. For the formation of the NiO RRAM nanocapacitor (Pt/NiO/graphene capacitor) array, an anodic aluminum oxide (AAO) nanotemplate with a pore diameter of about 30 nm and an interpore distance of about 100 nm was used. NiO and Pt were subsequently deposited on the graphene sheet. The NiO RRAM nanocapacitor had a diameter of about 30 ± 2 nm and a thickness of about 33 ± 3 nm. Typical unipolar switching characteristics of the NiO RRAM nanocapacitor array were confirmed. The NiO RRAM nanocapacitor array on graphene exhibited lower SET and RESET voltages than that on a bare surface of Nb-doped $SrTiO_3$.

KEYWORDS: resistive switching · NiO · nanocapacitor · graphene · anodizing aluminum oxide

Resistive random access memory (RRAM) is a feasible next generation, nonvolatile memory technology which utilizes two bistable resistances of high resistance states (HRS) and low resistance states (LRS).[1−6] Similar to the simple structure of dynamic random access memory (DRAM), one bit of RRAM memory can be composed of one transistor and one RRAM capacitor.[7,8] However, different from a DRAM capacitor, a RRAM capacitor exhibits two bistable resistances of HRS and LRS, which can be switched by an external bias or preserved as information for a long time. As a result, many researchers have extensively studied various RRAM dielectrics, from transition metal oxides to chalcogenides, which show two bistable resistances.[9−15] Since these various RRAM dielectrics can be more easily fabricated and handled than other memory media, such as ferroelectric materials, which require a high processing temperature for crystallization, RRAM memory is expected to be widely utilized for next generation nanoscale electronic devices.[16,17]

For the fabrication of nanoscale devices, it is necessary to form nanostructures of nanodots, nanotubes, and nanowires based on top-down or bottom-up approaches.[18−21] To provide small-sized nanostructures at a low cost, the bottom-up approach, which is mainly based on the self-assembly mechanism, is more promising for the fabrication of nanostructures than the top-down approach.[18] Various nanotemplates, such as anodic aluminum oxide (AAO), can be used as templates to form periodically patterned nanostructures.[22,23] These nanotemplates enable the formation of various nanostructures with a periodic pattern, and the interpore distance, pore diameter, and depth can be easily controlled.[23] Thus, nanotemplate-based nanostructure formation is a feasible technique for the production of nanoscale electronic devices.[24]

Recently, graphene has been actively researched due to its quantum electric transport, remarkably high mobility, high elasticity, and electromechanical modulation, similar to carbon nanotubes.[25−27] Graphene can be used as a transparent and flexible electrode and has demonstrated a very low sheet resistance and a high optical transparency.[27] Thus, it is expected that graphene is a good electrode, even for the fabrication of flexible nanoscale electronic devices. In this work, we fabricated a NiO RRAM nanocapacitor array containing an individual Pt top electrode on a graphene sheet attached to a Nb-doped $SrTiO_3$ substrate. The NiO RRAM nanocapacitors exhibited typical unipolar switching characteristics of a RRAM capacitor.

The schematic drawings for the fabrication of the NiO RRAM capacitor array structure on a graphene sheet are shown in Figure 1. AAO nanotemplates were prepared

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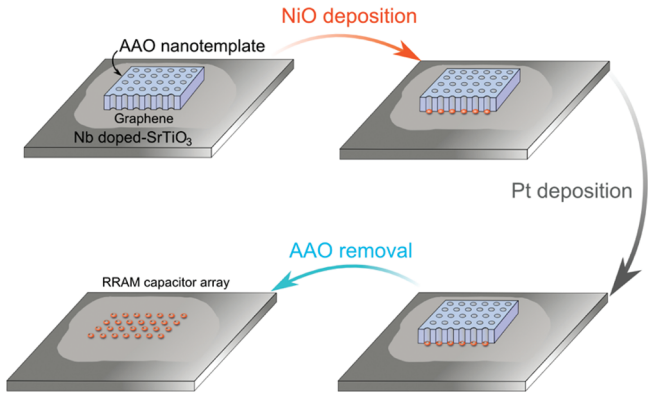

Figure 1. Schematic drawings of the fabrication of a NiO RRAM capacitor array on a graphene sheet: (a) an AAO nanotemplate is covered on a graphene sheet after the graphene sheet is attached to a Nb-doped $SrTiO_3$ substrate, (b) NiO deposition through the AAO nanotemplate, (c) Pt deposition on NiO nanodots in the AAO nanotemplate, and (d) the NiO RRAM nanocapacitor array after the removal of the AAO nanotemplate.

with a pore diameter of about 30 nm and an interpore distance of about 100 nm by four-step anodization of Al sheets, using 0.3 M oxalic acid at a constant anodization voltage of 40 V and a temperature of 15 °C.[23] As shown in the SEM image (Figure 2a), a good AAO nanotemplate was obtained with a long order. To make an atomically flat surface on the Nb-doped $SrTiO_3$ substrates (Nb doping level ~1 wt % and resistivity ~0.001 $\Omega \cdot$ cm), which can be used as a bottom electrode of a Pt/NiO/Nb-doped $SrTiO_3$ capacitor, as well as the interconnector of the graphene bottom electrode of a Pt/NiO/graphene capacitor, the Nb-doped $SrTiO_3$ substrates were dipped in a dilute HF solution and annealed at 1000 °C for 1 h.[28] The Nb-doped $SrTiO_3$ substrate had terraces with a uniform interval of about 100 nm and a very low roughness below 0.2 nm (Figure 2b). This smooth surface of the Nb-doped $SrTiO_3$ allows production of a smooth surface of the graphene sheet. After the Nb-doped $SrTiO_3$ substrate with an atomically smooth surface was prepared, graphene was added on the surface of the Nb-doped $SrTiO_3$ substrate exfoliated by mechanical cleavage from highly ordered pyrolytic graphite (HOPG), which is a periodic stack of two-dimensional graphene sheets along the *c* axis.[29] Then, the graphene sheet on the Nb-doped $SrTiO_3$ substrate was covered with an AAO nanotemplate, where the graphene sheet is utilized as a bottom electrode of a NiO RRAM capacitor. In this work, graphene sheets, which are excellent electrodes similar to metallic carbon nanotubes, were used as the bottom electrodes for the fabrication of NiO RRAM capacitors.[30] It is expected that the graphene sheets can reduce the SET and RESET bias voltages of RRAM capacitors because the work function of graphene (4.66 eV) is lower than that of noble metals, such as Pt.[30−32] An AAO membrane with a thickness of 400 nm was detached from the Al sheet in an ethanol/perchloric acid solution (4:1 ratio by volume) by applying a bias, and the AAO membrane then covered the surface of the graphene/Nb-doped $SrTiO_3$.[33] Through the AAO nanotemplate as a shadow mask, NiO and Pt were subsequently deposited by radio frequency (RF) sputtering. Finally, the NiO RRAM nanocapacitor array structure was obtained after the removal of the AAO nanotemplate. Figure 2c shows an atomic force microscope (AFM) image of the NiO RRAM nanocapacitor array on a graphene sheet after the removal of the AAO nanotemplate. The NiO RRAM nanocapacitor array also exhibits a well-arranged pattern, similar to the AAO nanotemplate. All NiO RRAM nanocapacitors had nearly uniform sizes. The terraces of the Nb-doped $SrTiO_3$ substrate can be vaguely observed below the arrow in Figure 2c, clarified by black dashed lines. The boundary of the graphene sheet on the Nb-doped $SrTiO_3$ substrate is indicated by a white dashed line. The resolution of the three-dimensional AFM image of the NiO RRAM nanocapacitors on a graphene sheet was magnified in Figure 2d. Each NiO RRAM nanocapacitor had a diameter of 30 ± 2 nm and a thickness of 33 ± 3 nm.

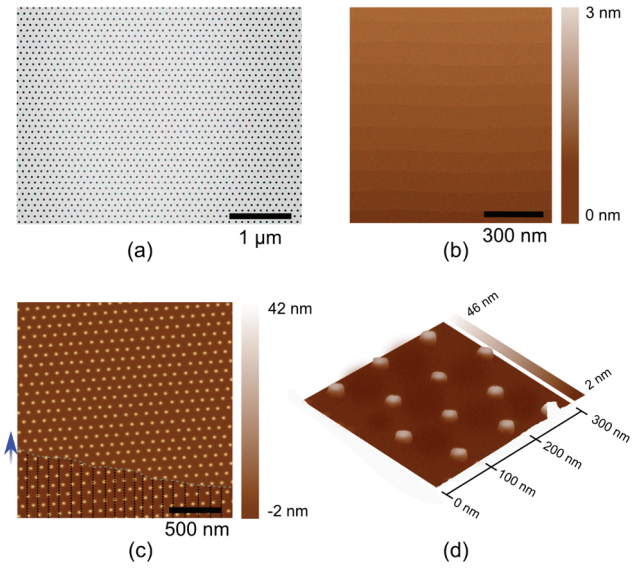

Figure 2. NiO RRAM nanocapacitor array on a graphene sheet. (a) SEM image of an AAO nanotemplate. The pores of the AAO nanotemplate show a well-ordered structure with a pore diameter of about 30 nm and an interpore distance of about 100 nm. (b) AFM image of the Nb-doped $SrTiO_3$ substrate. Well-arranged terraces are present with a uniform interval of about 100 nm. The Nb-doped $SrTiO_3$ substrate has an atomically smooth surface. (c) AFM image of the NiO RRAM nanocapacitor array on a graphene sheet. The arrow beside the AFM image indicates an edge of the graphene sheet. (d) Three-dimensional AFM image of the NiO RRAM nanocapacitor array from which a diameter of about 30 ± 2 nm and a thickness of about 33 ± 3 nm were obtained.

To verify the formation of the Pt top electrode on the NiO nanodot, the NiO RRAM nanocapacitors were observed by transmission electron microscopy (TEM), as shown in Figure 3a. Both the NiO nanodot and the Pt top electrode exhibited a polycrystalline structure. In particular, this image reveals the precise diameter and thickness of the NiO RRAM nanocapacitor. The thickness of the top Pt electrode was estimated to be about 5 nm.

For the NiO nanocapacitors, the currents as a function of applied voltage, resulting from the contact of a conducting Pt tip with the Pt top electrode of a NiO RRAM nanocapacitor, were measured (Figure 3b). The

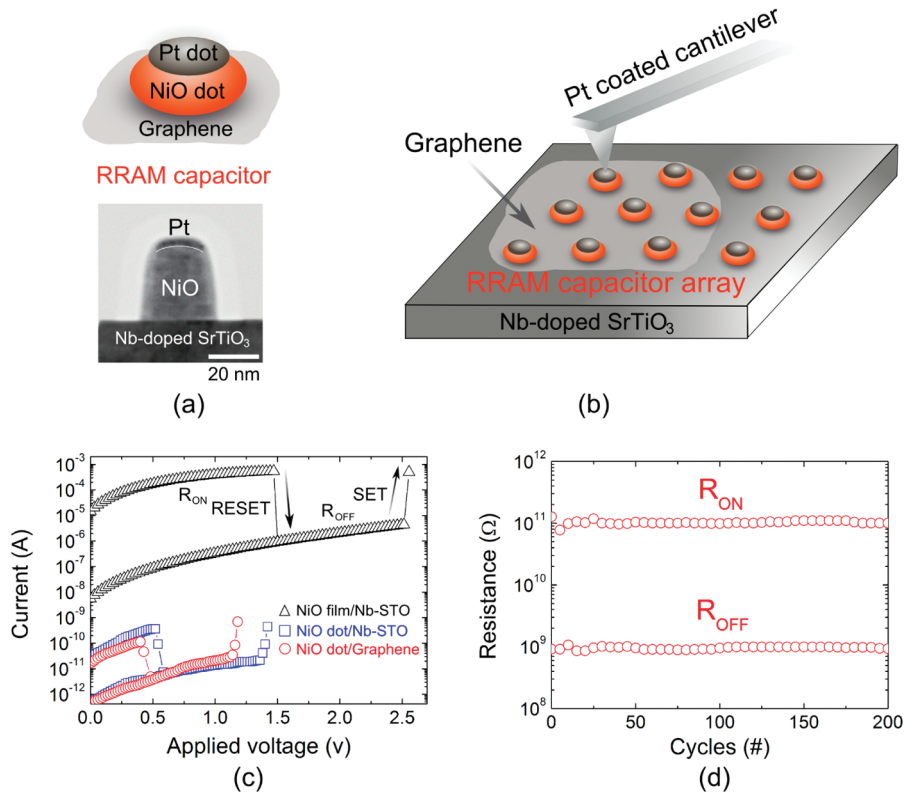

Figure 3. Switching characteristics of the NiO RRAM nanocapacitor array on a graphene sheet. (a) NiO RRAM nanocapacitor (Pt/NiO/graphene) and TEM image of a NiO nanocapacitor (Pt/NiO/Nb-doped $SrTiO_3$). (b) Electrical contact of a RRAM nanocapacitor with a Pt-coated cantilever. (c) Typical resistive switching characteristics of the NiO RRAM nanocapacitor on a graphene sheet and a Nb-doped $SrTiO_3$ substrate. The NiO RRAM nanocapacitor on graphene exhibited lower SET and RESET voltages than those on the surface of Nb-doped $SrTiO_3$. (d) Bistable resistivities as a function of switching cycle for a NiO RRAM nanocapacitor on a graphene sheet.

RRAM switching characteristics of NiO RRAM nanocapacitors on a graphene sheet or on a Nb-doped $SrTiO_3$ substrate with a NiO thin film capacitor were compared in Figure 3c.[34] These three NiO RRAM capacitors exhibited typical unipolar RRAM switching behaviors with a very low ON current below 1 nA. The SET voltage was about 1.5 V, and the RESET voltage was about 0.5 V for the two NiO RRAM nanocapacitors, while the SET and RESET voltages were 2.5 and 1.5 V for the NiO thin film capacitor. However, the NiO RRAM nanocapacitor on graphene had slightly lower SET and RESET voltages than those on the surface of Nb-doped $SrTiO_3$. Generally, SET and RESET voltages increase with the work function of electrodes, but well-defined Schottky contact between NiO and a graphene sheet causes a decrease of the SET and RESET voltages.[32] Thus, we suggest that the well-defined Schottky contact of NiO/graphene contributes to the lower SET and RESET voltages of the NiO nanocapacitor on graphene even though the work function of graphene (4.66 eV) is higher than that of Nb-doped $SrTiO_3$ (4.2 eV).[30−32] To verify the reproducible switching behavior of a NiO RRAM capacitor on a graphene sheet, bistable resistivities as a function of a switching cycle were obtained between SET and RESET at reading voltages of 0.8, 1.8, and 0.25 V (Figure 3d). Typical retention and endurance properties of the NiO RRAM capacitor were observed for up to 200 cycles with HRS and LRS, allowing the possibility for RRAM applications.

In summary, an anodic aluminum oxide (AAO) nanotemplate with a pore diameter of about 30 nm and an interpore distance of about 100 nm was used for the formation of the NiO RRAM nanocapacitor (Pt/NiO/graphene capacitor) array. The NiO RRAM nanocapacitor exhibited a diameter of about 30 ± 2 nm and a thickness of about 33 ± 3 nm. Typical unipolar switching characteristics of the NiO RRAM nanocapacitor array were confirmed. The NiO RRAM nanocapacitor array on graphene exhibited lower SET and RESET voltages than those on the surface of Nb-doped $SrTiO_3$.

METHODS

NiO RRAM Nanocapacitor Preparation and Measurements. Polycrystalline NiO thin films and Pt top electrodes were deposited on a graphene sheet on top of a Nb-doped $SrTiO_3$ substrate by a radio frequency sputtering method.[34] Commercially available 2 in. NiO and Pt targets were used for the deposition of the thin films that were at a base pressure of $\sim 10^{-7}$ Torr before deposition. During the NiO deposition, the working pressure of the gas mixture (argon and oxygen) was maintained at 10 mTorr at room temperature. The morphology and roughness of the NiO thin

film were observed by atomic force microscopy and transmission electron microscopy. To characterize the NiO RRAM nanocapacitors, atomic force microscopy was performed using a Pt-coated Si_3N_4 cantilever as a conducting AFM tip. The Pt-coated Si_3N_4 cantilever enabled contact to an external ampere meter with a Pt top electrode of an individual NiO RRAM nanocapacitor.

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REFERENCES AND NOTES

1. Beck, A.; Bednorz, J. G.; Gerber, C.; Rossel, C.; Widmer, D. Reproducible Switching Effect in Thin Oxide Films for Memory Applications. *Appl. Phys. Lett.* **2000**, *77*, 139–141.
2. Collier, C. P.; Mattersteig, G.; Wong, E. W.; Luo, Y.; Beverly, K.; Sampaio, J.; Raymo, F. M.; Stoddart, J. F.; Heath, J. R. A [2]Catenane-Based Solid State Electronically Reconfigurable Switch. *Science* **2000**, *289*, 1172–1175.
3. Watanabe, Y.; Bednorz, J. G.; Bietsch, A.; Gerber, C.; Widmer, D.; Beck, A.; Wind, S. J. Current-Driven Insulator-Conductor Transition and Nonvolatile Memory in Chromium-Doped $SrTiO_3$ Single Crystals. *Appl. Phys. Lett.* **2001**, *78*, 3738–3740.
4. Ouyang, J.; Chu, C.-W.; Szmanda, C. R.; Ma, L.; Yang, Y. Programmable Polymer Thin Film and Non-volatile Memory Device. *Nat. Mater.* **2004**, *3*, 918–922.
5. Green, J. E.; Wook Choi, J.; Boukai, A.; Bunimovich, Y.; Johnston-Halperin, E.; Delonno, E.; Luo, Y.; Sheriff, B. A.; Xu, K.; Shik Shin, Y.; Tseng, H.-R.; Stoddart, J. F.; Heath, J. R. A 160-Kilobit Molecular Electronic Memory Patterned at 1011 Bits per Square Centimetre. *Nature* **2007**, *445*, 414–417.
6. Lee, M.-J.; Seo, S.; Kim, D. C.; Ahn, S. E.; Seo, D. H.; Yoo, I. K.; Baek, I. G.; Kim, D. S.; Byun, I. S.; Kim, S. H.; Hwang, I. R.; Kim, J. S.; Jeon, S. H.; Park, B. H. A Low-Temperature-Grown Oxide Diode as a New Switch Element for High-Density, Nonvolatile Memories. *Adv. Mater.* **2007**, *19*, 73–76.
7. Bez, R. Innovative Technologies for High Density Non-volatile Semiconductor Memories. *Microelectron. Eng.* **2005**, *80*, 249–255.
8. Okhonin, S.; Nagoga, M.; Sallese, J. M.; Fazan, P. A Capacitor-Less 1T-DRAM Cell. *IEEE Electron Device Lett.* **2002**, *23*, 85–87.
9. Asamitsu, A.; Tomioka, Y.; Kuwahara, H.; Tokura, Y. Current Switching of Resistive States in Magnetoresistive Manganites. *Nature* **1997**, *388*, 50–52.
10. Mane, R. S.; Lokhande, C. D. Chemical Deposition Method for Metal Chalcogenide Thin Films. *Mater. Chem. Phys.* **2000**, *65*, 1–31.
11. Szot, K.; Speier, W.; Bihlmayer, G.; Waser, R. Switching the Electrical Resistance of Individual Dislocations in Single-Crystalline $SrTiO_3$. *Nat. Mater.* **2006**, *5*, 312–320.
12. Muenstermann, R.; Dittmann, R.; Szot, K.; Mi, S.; Jia, C.-L.; Meuffels, P.; Waser, R. Realization of Regular Arrays of Nanoscale Resistive Switching Blocks in Thin Films of Nb-Doped $SrTiO_3$. *Appl. Phys. Lett.* **2008**, *93*, 023110.
13. Son, J. Y.; Shin, Y. H.; Park, C. S. Bistable Resistive States of Amorphous $SrRuO_3$ Thin Films. *Appl. Phys. Lett.* **2008**, *92*, 133510.
14. Schindler, C.; Weides, M.; Kozicki, M. N.; Waser, R. Low Current Resistive Switching in Cu-SiO_2 Cells. *Appl. Phys. Lett.* **2008**, *92*, 122910.
15. Guan, W.; Liu, M.; Long, S.; Liu, Q.; Wang, W. On the Resistive Switching Mechanisms of Cu/ZrO_2:Cu/Pt. *Appl. Phys. Lett.* **2008**, *93*, 223506.
16. Chang, W.-Y.; Lai, Y.-C.; Wu, T.-B.; Wang, S.-F.; Chen, F.; Tsai, M.-J. Unipolar Resistive Switching Characteristics of ZnO Thin Films for Nonvolatile Memory Applications. *Appl. Phys. Lett.* **2008**, *92*, 022110.
17. Park, J.-W.; Park, J.-W.; Jung, K.; Yang, M. K.; Lee, J.-K. Influence of Oxygen Content on Electrical Properties of NiO Films Grown by RF Reactive Sputtering for Resistive Random-Access Memory Applications. *J. Vac. Sci. Technol., B* **2006**, *24*, 2205–2208.
18. Teichert, C. Self-Organization of Nanostructures in Semiconductor Heteroepitaxy. *Phys. Rep.* **2002**, *365*, 335–432.
19. Samuelson, L. Self-Forming Nanoscale Devices. *Mater. Today* **2003**, *6*, 22–31.
20. Xia, Y.; Yang, P.; Sun, Y.; Wu, Y.; Mayers, B.; Gates, B.; Yin, Y.; Kim, F.; Yan, H. One-Dimensional Nanostructures: Synthesis, Characterization, and Applications. *Adv. Mater.* **2003**, *15*, 353–389.
21. Barth, J. V.; Costantini, G.; Kern, K. Engineering Atomic and Molecular Nanostructures at Surfaces. *Nature* **2005**, *437*, 671–679.
22. Nicewarner-Pena, S. R.; Freeman, R. G.; Reiss, B. D.; He, L.; Pena, D. J.; Walton, I. D.; Cromer, R.; Keating, C. D.; Natan, M. J. Submicrometer Metallic Barcodes. *Science* **2001**, *294*, 137–141.
23. Lee, W.; Ji, R.; Gosele, U.; Nielsch, K. Fast Fabrication of Long-Range Ordered Porous Alumina Membranes by Hard Anodization. *Nat. Mater.* **2006**, *5*, 741–747.
24. Shingubara, S. Fabrication of Nanomaterials Using Porous Alumina Templates. *J. Nanopart. Res.* **2003**, *5*, 17–30.
25. Novoselov, K. S.; Geim, A. K.; Morozov, S. V.; Jiang, D.; Katsnelson, M. I.; Grigorieva, I. V.; Dubonos, S. V.; Firsov, A. A. Two-Dimensional Gas of Massless Dirac Fermions in Graphene. *Nature* **2005**, *438*, 197–200.
26. Li, X.; Wang, X.; Zhang, L.; Lee, S.; Dai, H. Chemically Derived, Ultrasmooth Graphene Nanoribbon Semiconductors. *Science* **2008**, *319*, 1229–1232.
27. Kim, K. S.; Zhao, Y.; Jang, H.; Lee, S. Y.; Kim, J. M.; Kim, K. S.; Ahn, J.-H.; Kim, P.; Choi, J.-Y.; Hong, B. H. Large-Scale Pattern Growth of Graphene Films for Stretchable Transparent Electrodes. *Nature* **2009**, *457*, 706–710.
28. Kawasaki, M.; Takahashi, K.; Maeda, T.; Tsuchiya, R.; Shinohara, M.; Ishiyama, O.; Yonezawa, T.; Yoshimoto, M.; Koinuma, H. Atomic Control of the $SrTiO_3$ Crystal Surface. *Science* **1994**, *266*, 1540–1542.
29. Ferrari, A. C.; Meyer, J. C.; Scardaci, V.; Casiraghi, C.; Lazzeri, M.; Mauri, F.; Piscanec, S.; Jiang, D.; Novoselov, K. S.; Roth, S.; Geim, A. K. Raman Spectrum of Graphene and Graphene Layers. *Phys. Rev. Lett.* **2006**, *97*, 187401.
30. Shan, B.; Cho, K. First Principles Study of Work Functions of Single Wall Carbon Nanotubes. *Phys. Rev. Lett.* **2005**, *94*, 236602.
31. Nagaraj, B.; Wu, T.; Ogale, S. B.; Venkatesan, T.; Ramesh, R. Interface Characterization of All-Perovskite Oxide Field Effect Heterostructures. *J. Electroceram.* **2002**, *8*, 233–241.
32. Seo, S.; Lee, M. J.; Kim, D. C.; Ahn, S. E.; Park, B. H.; Kim, Y. S.; Yoo, I. K.; Byun, I. S.; Hwang, I. R.; Kim, S. H.; Kim, J. S.; Choi, J. S.; Lee, J. H.; Jeon, S. H.; Hong, S. H. Electrode Dependence of Resistance Switching in Polycrystalline NiO Films. *Appl. Phys. Lett.* **2005**, *87*, 263507.
33. Lee, W.; Schwirn, K.; Steinhart, M.; Pippel, E.; Scholz, R.; Gosele, U. Structural Engineering of Nanoporous Anodic Aluminium Oxide by Pulse Anodization of Aluminium. *Nat. Nano* **2008**, *3*, 234–239.
34. Son, J. Y.; Shin, Y. H. Direct Observation of Conducting Filaments on Resistive Switching of NiO Thin Films. *Appl. Phys. Lett.* **2008**, *92*, 222106.